Journal of Basic and Applied Engineering Research
p-ISSN: 2350-0077; e-ISSN: 2350-0255; Volume 5, Issue 7; October-December, 2018, pp. 573-576

http://www.krishisanskriti.org/Publication.html

# Implementation of DHT Algorithm for a VLSI Architecture for Length N=32

**Deepti Gautam[1] and Anshuman Singh[2]**

*[1,2]Noida Institute of Engg. & Technology Greater Noida, U.P., India*
*E-mail: [1]deepti.gautam44@gmail.com, [2]anshumansingh1317@gmail.com*

**Abstract—***A new very large scale integration (VLSI) algorithm for a 2N-length discrete Hartley transform (DHT) that can be efficiently implemented on a highly modular and parallel VLSI architecture having a regular structure is presented. The DHT algorithm can be efficiently split on several parallel parts that can be executed concurrently[13]. Moreover, the proposed algorithm is well suited for the sub-expression sharing technique that can be used to significantly reduce the hardware complexity of the highly parallel VLSI implementation. With reduced complexity, ultimately the power consumption gets reduced and hence area also gets reduced [5]. In the proposed solution, we have used only multipliers with a constant that can be efficiently implemented in VLSI. The proposed solution is not only appealing by its high level of parallelism and by using a modular and regular structure but it can be also used to obtain a small hardware complexity by extensively sharing the common blocks.[14]*

*Here, we present a DHT algorithm for length N=32.*

**Keywords***: Discrete Hartley Transfrom (DHT), DHT domain processing, Discrete Fourier Transform (DFT).*

## 1. INTRODUCTION

Signal processing is a technology by which different form of signals is processed to represent these in various other forms as per application and use. Also, more advancement in electronic field major shift has been towards processing of digital signals. The concept of Parallel Processing in fastest growing VLSI technology greatly affects the modern day Signal Processing [3]. Use of parallel processing in VLSI implementation has advantages of fast speed and low power consumption. Although parallel processing leads to duplicity of many hardware architecture which increases cost but still we prefer parallel processing. Parallel processing requires multiple outputs which are computed in parallel in the same clock period and hence the sample speed is increased accordingly[2].

Discrete-time signal processing is actually done with computation of Fourier Transform which is called as Fast Fourier Transform. In Fourier analysis, signals are converted to/from frequency domain. The Fourier analysis of a periodic function is actually the extraction of series of sines-cosines when superimposed produces function. This whole analysis is represented in the form of Fourier series. Fast Fourier Transform (FFT) is a mathematical method for transforming a time-domain quantity into frequency domain quantity and vice-versa[10]. With FFT, the computation speed can be increased. It can be further increased by using DFT i.e. Discrete Fourier Transform [8].There are discrete orthogonal transforms which are basics of most of the image processing and signal processing applications. These are Discrete Cosine Transform (DCT), Discrete Fourier Transform (DFT), Discrete Hartley Transform (DHT) and Walsh-Hadamard Transform (WHT) [12]. DCT is mostly known for its very high energy compaction capability as it compacts most of the energy of a highly correlated signal into a small number of low-frequency transform co-efficient [7]. Due to this important property, the DCT has been adopted as part of many compression standards and used extensively in filtering, watermarking, encryption and orthogonal frequency division multiplexing (OFDM in short). However, DHT is extremely efficient alternative to DFT for real data [6]. Also, DHT has the properties of lower computational complexity, regularity and self-inverse. Due to these properties DHT is now been viewed as an increased interest in signal processing.[11]

The Discrete Hartley Algorithm, which is called as DHT in short, is proposed by Bracewell, [1] has become an important tool in image and signal processing. Discrete Hartley transform is nothing but also a form of Fourier Related Transform of discrete and periodic data similar to Discrete Fourier Transform. The main difference between the two lies in the fact that DHT transforms real inputs to real outputs and there is no involvement of complex numbers [9]. DHT plays a significant role in many DSP applications since it is a very efficient alternative to DFT for its real-number operations. Also inverse DHT is same as that of forward DHT except for scaling factor. Therefore, with this feature same program or same architecture can be used to carry out both the forward and inverse DHT calculations [4].

### 1.1 DHT Algorithm

#### 1.1.1 Basic Approach

To understand the meaning and implementation of DHT we have to first analyze it which is given below. Here the length is denoted by N.

Let N > 4 be a power of 2. For any real input sequence

{ x(i) } i = 0,1,2…..N - 1 }

DHT ( N ) is defined by

X(k) = DHT(N) { x(i) }

$= \sum_{i=0}^{N-1} x(i)$ . cas [2ki π / N]

for k = 0,1,2,3,4……..N-1 (1)

Where cas(x) = cos(x) + sin (x)

{ x(i) } i = 0,1,2…..N - 1 }

## 2. COMPUTATION OF N-LENGTH SEQUENCE: GENERALIZED EQUATIONS

We can compute an N-Length using a new algorithm given by the following relations:

$X_N$ (k) { x(i) } =

$X_{N/2}$ ( k) { x(2i) } + u (0) . sin (2k π / N) + [$X_{N/2}$ (k) { u(i) } – u (0) / 2]. 2. cos (2k π / N) (2)

$X_N$ (N/2 + k) { x(i) } =

$X_{N/2}$ ( k) { x(2i) } - u (0) . sin (2k π / N) - [$X_{N/2}$ (k) { u(i) } – u (0) / 2]. 2. cos (2k π / N) (3)

For k = 0,1,2,3……..N / 4 - 1

$X_N$ (N/2 - k) { x(i) } =

$X_{N/2}$ ( N/2 - k) { x(2i) } + u (0) . sin (2k π / N) - [$X_{N/2}$ (N/2 - k) { u(i) } – u (0) / 2]. 2. cos (2k π / N) (4)

$X_N$ (N - k) { x(i) } =

$X_{N/2}$ ( N/2 - k) { x(2i) } - u (0) . sin (2k π / N) + [$X_{N/2}$ (N/2 - k) { u(i) } – u (0) / 2]. 2. cos (2k π / N) (5)

For k = 0,1,2,3……..N / 4

Where

$X_{N/2}$ ( k) { x(2i) } = $\sum_{i=0}^{\frac{N}{2}-1} x(2i)$ . cas [ 2ki $\frac{\pi}{N/2}$ ] (6)

$X_{N/2}$ ( k) { u(i) } = $\sum_{i=0}^{\frac{N}{2}-1} u(i)$ . cas [ 2ki $\frac{\pi}{N/2}$ ] (7)

DHT of length N / 2 with { u(i) : i = 0,1,2…..N / 2 -1 }

An auxiliary input sequence given by

u (N /2 -1) = x (N-1) (8)

u (i) = x (2i + 1) – u (i + 1) (9)

for I = N/2 – 2, …..,1,0

We can further reduce the number of multipliers since we are multiplying with the same constant ‘c’. For the same purpose we can use same multiplier.

## 3. AUXILIARY INPUT SEQUENCES

The Implementation of DHT further involves use of some auxiliary input sequences. We first compute recursively auxiliary input sequences. $u^{(0)}$ , $v^{(0)}$ and $u^{(1)}$ comprises auxiliary input sequences which are given below. These equations are simple to understand in themselves and can be computed recursively [15]. To understand this let us consider DHT of length N = 32.

We first compute recursively auxiliary input sequences. $u^{(0)}$ , $v^{(0)}$ and $u^{(1)}$ comprises auxiliary input sequences which are given below:

$u^{(0)}$ (15) = x (31) (10)

$u^{(0)}$ (i) = x (2i + 1) - $u^{(0)}$ (i + 1) for i = 0,1,….14 (11)

$v^{(0)}$ (7) = x (30) (12)

$v^{(0)}$ (i) = x (4i + 2) - $v^{(0)}$ (7) (i + 1) for i = 0,1,….6 (13)

$u^{(1)}$ (7) = $u^{(0)}$ (15) (14)

$u^{(1)}$ (i) = $u^{(0)}$ (2i + 1) - $u^{(1)}$ (i + 1) for i = 0,1,….6 (15)

The above equations are obtained by further reformulation of the equations obtained directly from equations 2 to 5 in such a way that we can extensively use the technique of sub expression sharing and sharing the multipliers with the same constant [16]. Hence the number of multipliers has been reduced at only 16 which is significantly lower value.

## 4. DHT IMPLEMENTATION OF N=32

For $X_{32}$ (k),

$X_{32}$ (k) { x (i) } =

[$U_8$ (k) { x (4i) } + $U_8$ (k) { $v^{(0)}$ (i) } . 2 . cos (2k π / 16] +

x(0) / 2 + $v^{(0)}$ (0). sin (2k π / 16) + $u^{(0)}$ (0). sin (2k π / 32) +

[$U_8$ (k) { $u^{(0)}$ (2i) } + $U_8$ (k) { $u^{(1)}$ (i) }. 2. cos (2k π / 16)].2. cos (2k π / 32) + $u^{(1)}$ (0) . 2 sin (2k π / 16) . cos (2k π / 32)

(16)

$X_{32}$ (k+8) { x (i) } =

[$U_8$ (k) { x (4i) } - $U_8$ (k) { $v^{(0)}$ (i) } . 2 . cos (2k π / 16] +

x(0) / 2 - $v^{(0)}$ (0). sin (2k π / 16) + $u^{(0)}$ (0).cos (2k π / 32) -

[$U_8$ (k) { $u^{(0)}$ (2i) } - $U_8$ (k) { $u^{(1)}$ (i) }. 2. cos (2k π / 16)]. 2. cos (2k π / 32) + $u^{(1)}$ (0) .2 sin (2k π / 16) . sin (2k π / 32)

(17)

$X_{32}$ (16+k) { x (i) } =

$[U_8 (k) \{ x (4i) \} + U_8 (k) \{ v^{(0)} (i) \} . 2 . \cos (2k \pi / 16] +$
$x(0) / 2 + v^{(0)} (0). \sin (2k \pi / 16) - u^{(0)} (0). \sin (2k \pi / 32) -$
$[U_8 (k) \{ u^{(0)} (2i) \} + U_8 (k) \{ u^{(1)} (i) \}. 2. \cos (2k \pi / 16)]. 2. \cos (2k \pi / 32) - u^{(1)} (0) . 2 \sin (2k \pi / 16) . \cos (2k \pi / 32)$

(18)

$X_{32} (24+k) \{ x (i) \} =$
$[U_8 (k) \{ x (4i) \} - U_8 (k) \{ v^{(0)} (i) \} . 2 . \cos (2k \pi / 16] +$
$x(0) / 2 - v^{(0)} (0). \sin (2k \pi / 16) - u^{(0)} (0).\cos (2k \pi / 32) +$
$[U_8 (k) \{ u^{(0)} (2i) \} - U_8 (k) \{ u^{(1)} (i) \}. 2. \cos (2k \pi / 16)]. 2. \cos (2k \pi / 32) - u^{(1)} (0) . 2 \sin (2k \pi / 16) . \sin (2k \pi / 32)$

(19)

For k = 0,1,2,..3

$X_{32} (8-k) \{ x (i) \} =$
$[U_8 (8-k) \{ x (4i) \} - U_8 (8-k) \{ v^{(0)} (i) \} . 2 . \cos (2k \pi / 16] +$
$x(0) / 2 - v^{(0)} (0). \sin (2k \pi / 16) + u^{(0)} (0).\cos (2k \pi / 32) +$
$[U_8 (8-k) \{ u^{(0)} (2i) \} - U_8 (8-k) \{ u^{(1)} (i) \}. 2. \cos (2k \pi / 16)] .2.\sin (2k \pi / 32) + u^{(1)} (0) . 2 \sin (2k \pi / 16) . \sin (2k \pi / 32)$

(20)

$X_{32} (16-k) \{ x (i) \} =$
$[U_8 (8-k) \{ x (4i) \} + U_8 (8-k) \{ v^{(0)} (i) \} . 2 . \cos (2k \pi / 16] +$
$x(0) / 2 - v^{(0)} (0). \sin (2k \pi / 16) + u^{(0)} (0).\sin (2k \pi / 32) -$
$[U_8 (8-k) \{ u^{(0)} (2i) \} + U_8 (8-k) \{ u^{(1)} (i) \}. 2. \cos (2k \pi / 16)] . 2. \cos (2k \pi / 32) + u^{(1)} (0) . 2 \sin (2k \pi / 16) . \sin (2k \pi / 32)$

(21)

$X_{32} (24-k) \{ x (i) \} =$
$[U_8 (8-k) \{ x (4i) \} - U_8 (8-k) \{ v^{(0)} (i) \} . 2 . \cos (2k \pi / 16] +$
$x(0) / 2 + v^{(0)} (0). \sin (2k \pi / 16) - u^{(0)} (0).\cos (2k \pi / 32) -$
$[U_8 (8-k) \{ u^{(0)} (2i) \} - U_8 (8-k) \{ u^{(1)} (i) \}. 2. \cos (2k \pi / 16)] . 2. \sin (2k \pi / 32) - u^{(1)} (0) . 2 \sin (2k \pi / 16) . \sin (2k \pi / 32)$

(22)

$X_{32} (32-k) \{ x (i) \} =$
$[U_8 (8-k) \{ x (4i) \}+- U_8 (8-k) \{ v^{(0)} (i) \} . 2 . \cos (2k \pi / 16] +$
$x(0) / 2 + v^{(0)} (0). \sin (2k \pi / 16) - u^{(0)} (0).\sin (2k \pi / 32) +$
$[U_8 (8-k) \{ u^{(0)} (2i) \} + U_8 (8-k) \{ u^{(1)} (i) \}. 2. \cos (2k \pi / 16)] . 2. \cos (2k \pi / 32) - u^{(1)} (0) . 2 \sin (2k \pi / 16) . \cos (2k \pi / 32)$

(23)

For k = 1,2…4

A close examination of the respective equations for length N = 32 reveals that, some parameters are common to all the equations but only differ in process flow. These parameters can be prepared separately and later on can be implemented for their respective process flow.

## 5. FLOW DIAGRAM

Having implemented all the necessary blocks, now all of them can be complied up to create the final computation sequence of the DHT for N =32. The block diagram shows the flow

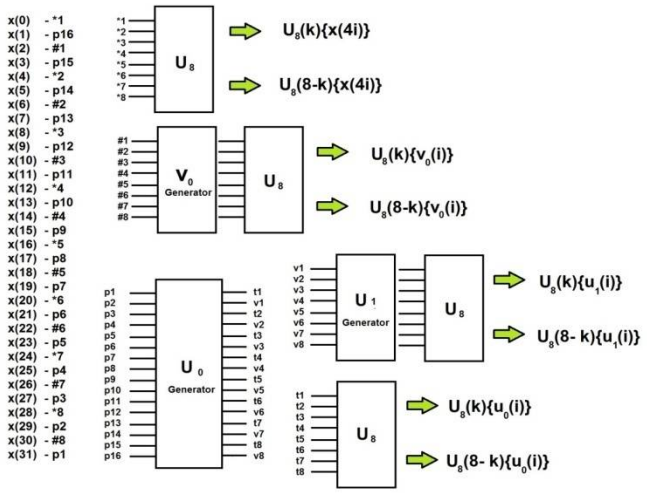


**Figure 1: Flow Diagram**

## 6. SYNTHESIS REPORT

Following is the synthesis report:

| Device Utilization Summary (estimated values) | | | [-] |
|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** |
| Number of Slice LUTs | 2437 | 46560 | 5% |
| Number of fully used LUT-FF pairs | 0 | 2437 | 0% |
| Number of bonded IOBs | 595 | 360 | 165% |
| Number of DSP48E1s | 17 | 288 | 5% |

**Figure 2; Synthesis Report**

Also following is the reported Hardware Utilization occurred, extracted from the Synthesis Report Logs.

```
=========================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                          : 6
 8x6-bit single-port distributed Read Only RAM  : 6
# MACs                                          : 14
 10x8-to-18-bit Mult with pre-adder             : 8
 18x8-to-26-bit Mult with pre-adder             : 4
 9x7-to-19-bit MAC                              : 2
# Multipliers                                   : 7
 28x8-bit multiplier                            : 4
 9x7-bit multiplier                             : 1
 9x9-bit multiplier                             : 2
# Adders/Subtractors                            : 143
 10-bit adder                                   : 16
 10-bit subtractor                              : 8
 11-bit adder                                   : 12
 11-bit subtractor                              : 12
 12-bit adder                                   : 8
 12-bit subtractor                              : 12
 17-bit adder                                   : 8
 17-bit subtractor                              : 4
 18-bit adder                                   : 1
 18-bit subtractor                              : 5
 20-bit adder                                   : 2
 20-bit subtractor                              : 2
 28-bit adder                                   : 4
 28-bit subtractor                              : 4
 37-bit adder                                   : 4
 37-bit subtractor                              : 4
 38-bit adder                                   : 8
 9-bit subtractor                               : 29
# Multiplexers                                  : 16
 17-bit 2-to-1 multiplexer                      : 12
 17-bit 4-to-1 multiplexer                      : 4

=========================================================
```

**Figure 3; Adv. HDL Synthesis Report**

## 7. CONCLUSION

Since the computation of DHT of length N = 32 is computationally very extensive also, if each input sequence is taken to be of length 8 bits, then it will lead to the occupation of a large number of I/O pins of an FPGA. Thus under such conditions, it is highly desirable that the inputs be taken serially through means of some SERIAL PROTOCOL medium and then be assigned in the FPGA.

The application of this algorithm leads to less hardware complexity and hence power consumption also gets reduced which remains a major concern while dealing with VLSI circuits. DHT algorithm implements sub-sharing expression technique and sharing of multipliers which are having same constants. DHT is most useful to use in signal processing and image compression applications.

## REFERENCES


[1] Doru Florin Chiper, *Senior Member, IEEE* "A novel VLSI DHT algorithm for a highly parallel and modular architecture" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 60, Issue 5, MARCH 2013.

[2] Doru Florin Chiper, *Senior Member, IEEE* "Radix-2 Fast Algorithm for Computing Discrete Hartley Transform of Type III" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 59, NO. 5, MAY 2012

[3] Michela Svaluto Moreolo, Raül Muñoz, and Gabriel Junyent "Novel Power Efficient Optical OFDM Based on Hartley Transform for Intensity-Modulated Direct-Detection Systems "JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 28, NO. 5, MARCH 1, 2010

[4] Chin-Kuo Jao, Syu-Siang Long, and Muh-Tian Shiue, *Member, IEEE* "DHT-Based OFDM System for Passband Transmission Over Frequency-Selective Channel "IEEE SIGNAL PROCESSING LETTERS, VOL. 17, NO. 8, AUGUST 2010

[5] Saad Bouguezel, M. Omair Ahmad, *Fellow, IEEE*, and M. N. S. Swamy, *Fellow, IEEE* "New Parametric Discrete Fourier and Hartley Transforms, and Algorithms for Fast Computation "IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 58, NO. 3, MARCH 2011

[6] Based Real-Valued Discrete Gabor Transform "IEEE TRANSACTIONS ON IMAGE PROCESSING, VOL. 21, NO. 7, JULY 2012

[7] Liang Tao and Hon Keung Kwan, *Senior Member, IEEE* "Multirate-Based Fast Parallel Algorithms for 2-D DHT-Pramod Kumar Meher, *Senior Member, IEEE*, Thambipillai Srikanthan, *Senior Member, IEEE*, and Jagdish C. Patra, *Member, IEEE* "Scalable and Modular Memory-Based Systolic Architectures for Discrete Hartley Transform "

[8] IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 53, NO. 5, MAY 2006

[9] G. Eason, B. Noble, and I.N. Sneddon, "On certain integrals of Lipschitz-Hankel type involving products of Bessel functions," Phil. Trans. Roy. Soc. London, vol. A247, pp. 529-551, April 1955. (*references*)

[10] J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.

[11] I.S. Jacobs and C.P. Bean, "Fine particles, thin films and exchange anisotropy," in Magnetism, vol. III, G.T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271-350.

[12] R. Nicole, "Title of paper with only first word capitalized," J. Name Stand. Abbrev., in press.

[13] Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interface," IEEE Transl. J. Magn. Japan, vol. 2, pp. 740-741, August 1987 [Digests 9th Annual Conf. Magnetics Japan, p. 301, 1982].

[14] M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.

[15] Michela Svaluto Morelo, Member, IEEE 'Performance Analysis of DHT-based Optical OFDM Using Large-Size Constellations in AWGN 'IEEE COMMUNICATIONS LETTERS, VOL. 15, NO.5, MAY 2011.

[16] [16] Huazhong Shu, *Senior Member, IEEE*, JiasongWu,

[17] *Member, IEEE*, Chunfeng Yang, and Lotfi Senhadji, *Senior Member, IEEE* "Fast Radix-3 Algorithm for the Generalized Discrete Hartley Transform of Type II "IEEE SIGNAL PROCESSING LETTERS, VOL. 19, NO. 6, JUNE 2012